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Citation: J. Appl. Phys. 111, 114513 (2012); doi: 10.1063/1.4729030
View online: http://dx.doi.org/10.1063/1.4729030
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v111/i11
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Fabrication and characterization of InAlN/GaN-based double-channel high electron mobility transistors for electronic applications

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(Received 8 May 2012; accepted 9 May 2012; published online 12 June 2012)

In our previous work [J. S. Xue et al., Appl. Phys. Lett. 100, 013507 (2012)], superior electron-transport properties are obtained in InAlN/GaN/InAlN/GaN double-channel (DC) heterostructures grown by pulsed metal organic chemical vapor deposition (PMOCVD). In this paper, we present a detailed fabrication and systematic characterization of high electron mobility transistors (HEMTs) fabricated on these heterostructures. The device exhibits distinct DC behavior concerning with both static-output and small-signal performance, demonstrating an improved maximum drain current density of 1059 mA/mm and an enhanced transconductance of 223 mS/mm. Such enhancement of device performance is attributed to the achieved low Ohmic contact resistance as low as 0.33 ± 0.05 Ω mm. Moreover, very low gate diode reverse leakage current is observed due to the high quality of InAlN barrier layer deposited by PMOCVD. A current gain frequency of 10 GHz and a maximum oscillation frequency 21 GHz are also observed, which are comparable to the state-of-the-art AlGaN/GaN-based DC HEMT found in the literature. The results demonstrate the great potential of PMOCVD for application in InAlN-related device’s epitaxy.

I. INTRODUCTION

AlGaN/GaN-based high electron mobility transistors (HEMTs) continue to receive widespread research and development efforts, since the first HEMT was demonstrated two decades ago.1 However, recently, lattice-matched InAlN/GaN heterostructures have been extensively studied as one of the most promising alternatives to commercially already available AlGaN/GaN-based HEMTs upon the predication from theoretical calculation by Kuzmik,2 whose attractive prospects can dramatically alleviate the deleterious effects of built-in misfit strain induced defects on carrier density and mobility in nitride heterostructures.3,4 Lattice-matched InAlN/GaN heterostructures are free of strain, which reduces strain-defects related relaxation problems, resulting in better reliability and repeatability existing in highly inherent mismatched AlGaN/GaN heterostructures. Also, higher sheet carrier density can be induced by the large polarization discontinuity and band offset between InAlN barrier and GaN channel even without the contribution from piezoelectric polarization, providing higher output current density and better power performance.5 Furthermore, thin InAlN barrier enables fabrication of highly scaled devices while maintaining sufficiently high aspect ratio and effectively suppressing short channel effects, which reduces the technical difficulties and improves uniformity across the wafer by avoiding the damage caused by recess process on the channel. In addition, a high thermal and chemical stability has been demonstrated for lattice-matched InAlN/GaN HEMT, and devices operate up to 1000°C without showing serious performance degradation.6

Motivated by these potential advantages mentioned above, significant progress with respect to device performance and structure has been achieved with this new InAlN/GaN heterostructures during last five years. Alomari et al.5 reported a maximum drain current density of 2.4 A/mm in device with thermally generated oxide recess, while Wang et al.7 demonstrated a transconductance exceeding 800 mS/mm in enhancement-mode device. A current gain cutoff frequency of 300 GHz has been obtained in 30 nm gate length device with InGaN back barrier,8 while an output power density of 10.3 W/mm with a power added efficiency of 51% has been realized at 10 GHz for a 250 nm gate length device.9 Besides, excellent N-polar device performance has also been achieved.10 Moreover, terahertz detectors can also benefit from it.11 Despite these outstanding results, studies on InAlN/GaN double-channel (DC) HEMTs are sparse up to now due to the challenge in material growth, even though DC HEMTs have been successfully applied to AlGaN/GaN heterostructures.12 Therefore, it is of interest to fabricate DC HEMTs utilizing the superiority of lattice-matched InAlN/GaN heterostructures. A prerequisite for a monolithic approach to the realization of such devices is high quality epitaxial DC InAlN/GaN heterostructures. Fortunately, our group has successfully overcome the growth impediment by using pulsed metal organic chemical vapor deposition (PMOCVD),13–16 an inspiring method and facilitating the InAlN material-related applications. Here, we report on a detailed fabrication and characterization of HEMTs made of those DC InAlN/GaN heterostructures for electronic applications like frequency multipliers and mixers. We do recognize this demonstration as a first based on InAlN material.

http://dx.doi.org/10.1063/1.4729030

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II. EPITAXIAL GROWTH AND DEVICE FABRICATION

Figure 1 shows a schematic diagram of fabricated InAlN/GaN DC HEMT, which was grown on a 2-in c-plane sapphire substrate by PMOCVD at Xidian University. The epitaxial structure is composed of, from the substrate up, a 1.6 μm GaN buffer layer, a 1 nm AlN interlayer, a 12 nm InAlN bottom barrier layer, a 20 nm GaN layer, a 1 nm AlN interlayer, and a 12 nm InAlN top barrier layer. All of the layers are unintentionally doped. Details of layers’ epitaxy have been reported in a recent publication. The indium composition of two InAlN barriers is determined to be approximate 17% by high-resolution x-ray diffraction, reproducing the previously reported results. Room-temperature (RT) Hall effect measurements, conducted on a 1 cm × 1 cm sample in van der Pauw geometry using four indium dots as Ohmic contacts, produced a sheet carrier density of \( 10^{13} \text{ cm}^{-2} \) with an electron mobility of 1289 cm²/V·s, yielding a sheet resistance \( (R_{\text{sh}}) \) of 244 Ω/sq. Capacitance voltage characterization (not shown here) indicates good electron transport properties with DC behavior.

The DC HEMTs were prepared by the following fabrication procedures, and process control monitor (PCM) and transmission line method (TLM) structures were present to monitor material parameters. Ohmic contacts of Ti/Al/Ni/Au (220/1400/550/450 Å) metal stacks were firstly deposited by electron beam evaporation, and annealed with rapid thermal annealing system at 830°/C. Then, a gate electrode was deposited by electron beam evaporation. The buffer leakage current was measured as low as 25 nA/mm between two 100 μm wide isolated mesas separated by 5 μm. The \( R_{\text{sh}} \) and ohmic contact resistance \( (R_c) \) revealed by postprocess TLM measurements were 347 ± 20 Ω/sq and 0.33 ± 0.05 Ω·mm, respectively. This \( R_{\text{sh}} \) value is higher than that extracted from Hall measurements on as-grown material. As electrical properties of two dimensional electron gas (2DEG) and surface morphology of InAlN barrier could be characterized after Ohmic contact process, the physical mechanism behind this inconsistency in the electrical properties of the 2DEG is not well understood at present. It might be related to a difference in the quality of Ohmic contacts or a modification of the potential of the bare InAlN surface during the various device processing steps. It may be also related to some nonuniformity of the sample, and TLM result for the small area is higher than average Hall effect measurement across the large wafer. Compared to previously reported results on high-Al-content InAlN material,\(^{17}\) a relatively low \( R_c \) is achieved, which is critical for the performance of any HEMT in general, and InAlN-based HEMT in particular. Later, 100 nm SiN passivation was achieved by plasma-enhanced chemical vapor deposition to reduce frequency dispersion. The sheet resistance of the layer after passivation measured by TLM structures was 230 ± 20 Ω/sq, which is consistent with the Hall measurement on as-grown wafer. The realized reduction in sheet resistance is indicative of effective surface passivation.\(^{18}\) A gate length \( (L_G) \) of 0.8 μm was defined by standard photolithography after opening of gate area by etching the top SiN using CF₄ plasma. Finally, a Ni/Au/Ni (450/2000/200 Å) gate electrode was deposited by electron beam evaporation. All devices studied in this work have a gate width of 2 × 50 μm, a gate-source spacing of 0.7 μm, and a gate-drain spacing of 2.5 μm.

III. RESULTS AND DISCUSSION

The representative dc current-voltage (I-V) characteristics for an InAlN/GaN DC HEMT are described in Fig. 2. The drain-source voltage \( (V_{DS}) \) was swept up to +10 V, and the gate-source \( (V_{GS}) \) voltage was stepped from +2 to −10 V in −2 V increments. The maximum drain current density of \( 1059 \text{ mA/mm} \) was obtained at \( V_{DS} = 7 \text{ V} \) and \( V_{GS} = 2 \text{ V} \). A poor control of electrons in lower channel gives rise to an evident kink effect on I-V curves at \( V_{GS} = 0 \) and −2 V, which is indicative of strong dependence of the series resistance of the lower channel on the drain bias.\(^{12}\) At large drain biases and high current levels, a slight reduction of current along with negative differential resistance in saturation region is visible due to the self-heating effect caused by the poor thermal conductivity of the sapphire substrate, which can be ameliorated by adopting SiC substrate. The obtained performance, although rather conservative compared to the conventional single channel HEMTs in the current density and transconductance, confirms the presence of high density 2DEG channel and is ascribed to the limited device process considering the gate dimensions used in this work. It points to the need for further enhancement of drain current density employing reduced device dimensions.

FIG. 1. Cross-sectional schematic diagram of fabricated InAlN/GaN DC HEMT.

FIG. 2. Typical drain current-voltage characteristics of an InAlN/GaN DC HEMT.
complete channel pinchoff is not possible at higher drain biases of $V_{DS} = 8$ V and $V_{GS} = -6$ V, and a residual gate current $I_{GD}$ of 10 $\mu$A/mm flows through the gate while drain current $I_{DS}$ is 31 mA/mm. Given the good isolation between mesas associated with low buffer leakage current as mentioned previously, the leakage current through buffer layer and gate diode can be excluded as the reasons for the soft pinchoff. We attribute it to the efficient access to the lower carrier channel under larger drain bias.

Figure 3 presents the transfer characteristics of the same device at $V_{DS} = 10$ V. The device exhibits a maximum extrinsic transconductance of 223 mS/mm at $V_{GS} = 0.3$ V. However, another transconductance peak of 130 mS/mm is observed at $V_{GS} = -5.2$ V. The two peaks appearing in the curve of transconductance dependence on gate bias $V_{GS}$ obviously reflect the DC behavior of the fabricated HEMT, which correspond to the upper and the lower 2DEG channels modulated by different gate voltages. These properties are superior to values previously reported for similar structures based on AlGaN/GaN heterostructures. 19 Here, a better dc characteristic is realized on sample with slight inferior electric properties in comparison with the early reported,15 which is ascribed to highly desirable low Ohmic contact resistance since it generally dominates the total parasitic resistance. The extrapolated threshold voltage ($V_{T}$) was $-6.5$ V. Such a high $V_{T}$ value is attributed to the high 2DEG density in the channel as well as the relatively increased separation between gate and lower channel. The three-terminal breakdown voltage performed by biasing the gate at $V_{GS} = -9$ V and sweeping $V_{DS}$ until $I_{DS} = 1$ mA/mm is found to be 16 V. The actual (destructive) breakdown voltage happens between the gate and drain at $V_{DS} = 26$ V. The question of breakdown voltage requires further investigation to clarify its physical origin.

Figure 4 shows a typical gate leakage current curve of Ni/Au/Ni Schottky diode contacts on InAlN/GaN DC HEMTs at RT. Schottky-contact parameters were extracted from the forward I-V curve by linear fitting based on the thermionic emission model. The calculated values of Schottky barrier height and ideality factor were 0.84 eV and 1.51, respectively. Such barrier height obtained is close to the reported value of 0.75 eV measured by Arslan et al.,20 but significantly lower than 1.46 eV evaluated by Donoval et al.31 and 2.36 eV predicted for commonly used Ni contact on lattice-matched InAlN/GaN considering known work function of the metal and InAlN.22 According to the reverse I-V curve, the device exhibits remarkably minimal gate diode reverse leakage current on the order of 1 and 40 $\mu$A/mm at gate-drain voltage of $V_{GD} = -10$ and $-20$ V, respectively. This very low leakage is linked to high-insulating GaN buffer and high quality Schottky diode as well as absence of defects into the upper InAlN barrier layer resulting from high growth quality by PMOCDV, as revealed that the gate reverse-bias leakage current is associated with dislocations in the InAlN barrier layer.33 As shown in Fig. 4, when the device is pinched off below $-7$ gate bias, the drain leakage current is dominated by reverse-biased gate current, and no leakage current through the buffer is observed, which is in agreement with the device process result and a proof of high-resistive GaN buffer.

Pulsed I-V measurements were performed at quiescent bias points of $(V_{GS}, V_{DS}) = (0 \text{ V}, 0 \text{ V})$ using a 500 ns pulse length and a 1 ms period. Meanwhile, dc I-V output characteristics of the same HEMT were provided for comparison. During the measurement, the gate bias was changed from 2 to $-10$ V in 3 steps, and the drain bias was swept from 0 to 10 V. Zero gate and drain voltage were chosen as the initial bias point for each pulse to highlight the effect of self-heating, which is illustrated as a higher output conductance at the pulse condition than that at the dc condition (Fig. 5).
The thermal effect is more evident from the pulse data, and the drain current densities pulsed from \((V_{GS}, V_{DS}) = (0, 0)\) are higher than that at dc, indicating that the device suffers from self-heating under dc operation. As expected, the pulsed drain current density increases to 1287 mA/mm at a gate bias voltage of 2 V.

The RF small-signal performance of the transistor was also investigated by measuring \(S\)-parameters from 100 MHz to 40 GHz at a variety of bias points by using an Agilent E8363 vector network analyzer. Figure 6(a) shows the plots of short circuit current gain \(h_{21}\) and Mason’s unilateral gain \(U\) against frequency at the optimum bias points of \(V_{DS} = 10\) V and \(V_{GS} = -5.2\) V. A unity current gain cutoff frequency \(f_T\) of 10 GHz and a maximum oscillation frequency \(f_{MAX}\) of 21 GHz were obtained by extrapolating measured data with a slope of \(-20\) dB/s using a least square fit. The frequency performance can be further improved by scaling down the device gate length. DC behavior is also observed in the dependence of \(f_T\) and \(f_{MAX}\) on \(V_{GS}\) as depicted in Fig. 6(b), where \(V_{DS}\) was varied while keeping \(V_{DS}\) identical to that used for the measurements of maximum \(f_{MAX}\)’s. The variations in measured frequencies can be explained by the change of channel resistance and drift velocity of channel electrons when electrons populate the lower and upper channels in sequence, as \(V_{GS}\) increases from pinchoff voltage to higher values.\(^{19}\)

In contrast to the mature fabrication technology for AlGaN/GaN device, there still exists large room to further improve the device performance of InAlN/GaN-based DC HEMT, and future results are sure to surpass our reported parameters here. As another application, DC HEMTs provide more degree of freedom to tailor the gain linearity as demonstrated by T. Palacios et al.\(^{24}\) Due to the very high potential barrier between two channels, the results do not show any improvement in linearity with regard to the standard single channel device. The transconductance response could be made flat corresponding to the gate voltage by an appropriate structure design. We are looking more carefully into the design aspect of this material structure for next version of this device to improve it. Moreover, doping should be introduced to achieve high sheet carrier density and maintain a low energy barrier for carrier transfer between channels.\(^{25}\) An additional factor affecting the performance is the relatively large gate length, which should be further scaled down using more advanced technology like electron beam lithograph.

**IV. CONCLUSIONS**

In summary, InAlN/GaN DC HEMTs grown through PMOCD on sapphire substrate with distinct DC behavior have been demonstrated and characterized. It is suggested that a correct and proper design of material structure is of great importance to increase the linearity of both transconductance and cutoff frequency versus drain current in DC HEMTs. Further improvements are expected through the optimization of epitaxial structures, such as composition graded bottom InAlN barrier layer, and improvements in device processing technology, such as scaling down the gate length. Although the linearity needs to be improved, the overall device performance demonstrates the great potential of InAlN-based HEMTs for electronic applications including millimeter-wave power electronics and integrated digital circuits such as frequency multiplier and mixer at the moment the technology matures. Additionally, as evidenced, PMOCD provides a new route for InAlN-related electronic devices’ epitaxy, and can be also applied in growth of optoelectronic structures like distributed Bragg reflectors.

**ACKNOWLEDGMENTS**

This work was supported by the National Key Science and Technology Special Project (Grant No. 2008ZX01002-002), the Major Program and State Key Program of National Natural Science Foundation of China (Grant Nos. 60890191 and 60736033).

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