A Hardware Accelerate Simulator for Network Processor Based on FPGA
Zhixiong Di\textsuperscript{1,a}, Kang Li\textsuperscript{2,b}, Jie Pang\textsuperscript{3,c}, Jiangyi Shi\textsuperscript{4,d}, Peijun Ma\textsuperscript{5,e}, Yue Hao\textsuperscript{6,f}
\textsuperscript{1,2,3,4,5,6} School of Microelectronics, XiDian University, Xi’an 710071, China
\textsuperscript{a} zxdi@mail.xidian.edu.cn

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Abstract. With the dramatically increase of the scale of the Network Processor, traditionally verification method can't satisfied the requirement of market due to the limitation of the simulate speed. For solving the verification problems, a novel hardware accelerate simulator for Network Processor based on FPGA is proposed. This simulator improves the simulate speed remarkably. Furthermore, the probed signals of the Network Processor can be dumped into wave file real-timely.

Introduction
With the fast development of the Internet, the network processor plays a more and more important role in the network system. In order to deal with the various Internet protocol and relieve the pressure brought by the increasing bandwidth, the structure of the network processor is becoming more and more complex. Meanwhile, it is difficult to verify through the traditional simulate technology.

Challenges
The traditional simulate technology based on the EDA tools is perfect in debugging that all internal signals in designs can been seen distinctly to the engineers. But a low efficiency has been resulted in by the lengthiness simulate time. Thus it is not suitable for the verification of the network processor. Recent years, some prototype verification platforms, such as VStation, HES, and Palladium, have been proposed and applied into the verification flow successfully. These prototype platforms can perform as fast as the real circuits. More important is that all the signals in circuits can be probed which contribute a lot to accelerate the verification process. However, these platforms are too expensive to afford for most design teams. Besides, some software and hardware co-simulation have been proposed in paper[1-4], but it required a software model to the hardware which is too complicated to implementation for the SoC design. Paper[5] has proposed a hardware simulation scheme, nevertheless, a EDK platform must be built.

Upon the above researches, a novel hardware accelerate simulator for Network Processor based on FPGA is presented in this paper. Through this simulator the time consumed by the verification of the Network Processor is much shorter than it by using the EDA tools, such as Modelsim6.5b or NC-Verilog.

Overview of the Network Processor
Figure1 is a simplified block diagram of the Network Processor which shows the several main functional units.

![Fig.1 The architecture of the Network Processor](image-url)
As is shown in the Fig. 1, the package processors can be used for any function requiring high-speed packet inspection, data manipulation, and data transfer. The data bus, which is controlled by the package processors, takes charge of the data packages communication between the network processor and Ethernet MACs.

**Proposed Hardware Accelerate simulator Architecture**

**Overview of the Architecture**

Shown in Fig.2, the proposed hardware accelerate simulator employs Xilinx Vertex4 platform.

![Fig.2 The architecture of the proposed simulator](image)

On the simulate platform, the data communication between the Network Processor, the MACs and the PC is controlled by the PowerPC core. The PowerPC core is responsible for scheduling the data packages propagation direction between the MACs and the Network Processor. In addition, the PowerPC records the value of the critical signals and dumps them to the PC in the wave file.

In the simulate process, USB interface is used to as the data transform channel to connect PC and the simulate platform. Besides it is also used to transmit the value of the monitoring signals to PC so as to real-time monitor the simulate process. The MAC block on the platform is a timing generator act as a real MAC device.

**Scheduling mechanism**

On the proposed simulate platform, all the working parts is controlled by the PowerPC core. The data flow in the simulate process is shown in the Fig.3 and Fig.4.

![Fig.3 NP receive packages](image)  ![Fig.4 NP transmit packages](image)

In the process of the Network Processor receive data packages, PowerPC core receive the packages from the PC through the USB interface. Subsequently the PLB bus is operated by the PowerPC to transmit those packages to the specified MAC. Eventually, the Network Processor receive the packages from the MAC and written back to the PC. By comparing the receive packages and the transmit packages, whether the communication between the Network Processor and the specified MAC successfully can be asserted.

Likewise, when the Network Processor is in the transmit state, PowerPC core receive the data packages from the PC and retransmit them to the Network Processor through the PLB bus. Finally PowerPC core read the data packages from the specified MAC and write back to the PC.

**Probe mechanism**
In order to monitor the operation conditions of the Network Processor, the PowerPC core records the probed signals and feedback to the PC. For alleviating the pressure of the PLB bus, saving bus bandwidth, and reducing response time, the quantity of probed data is reduced greatly by the probe mechanism. By adopting this mechanism, only on the condition that the value of the probed signals changes, does the records procedure occur. Through this mechanism, the size of probed data can reduced greatly from several gigabits to a few megabit, compared the way that those signals is gathered each clock cycle. Moreover, in order to keep compatible with the EDA tools, the value of these probed signals are written in the file format of *.v. Thus, the wave of these signals can be view using the EDA tools. By checking this recorded information of simulate process, errors can be located easily.

**Experimental Results**

The proposed hardware accelerate simulator is implemented with the virtex4 FPGA device. The resource consumption of this simulator architecture is illustrated in Table 1. For testing the simulate speed more rigorously, data packages of various size are given on this proposed simulator platform. The relation between the simulate time and the size of the packages is demonstrated in the Table 2. Moreover the waveform of the probed signals shown in Fig.5 indicates the Network Processors can communicate with Ethernet MACs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulator</th>
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<tbody>
<tr>
<td>Number of Slices</td>
<td>22934</td>
</tr>
<tr>
<td>Number of Flip Flops</td>
<td>15085</td>
</tr>
<tr>
<td>Number of LUTs</td>
<td>36228</td>
</tr>
<tr>
<td>Number of BRAMs</td>
<td>86</td>
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<tr>
<td>Frequency</td>
<td>123.4MHz</td>
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</table>

<table>
<thead>
<tr>
<th>Data packages size</th>
<th>EDA tools (hour)</th>
<th>Proposed simulator (minute)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1M</td>
<td>1.2</td>
<td>0.01</td>
</tr>
<tr>
<td>10M</td>
<td>11.6</td>
<td>0.15</td>
</tr>
<tr>
<td>20M</td>
<td>28.3</td>
<td>1.3</td>
</tr>
<tr>
<td>100M</td>
<td>167.4</td>
<td>9.6</td>
</tr>
</tbody>
</table>

**Summary**

In this paper, a novel hardware accelerate simulator for Network Processor based on FPGA is proposed. By adopting the scheduling mechanism, the transfer flow of data packages between the network processor can be verified more easily than traditional FPGA verification method. Furthermore through the probe mechanism, the probed signals can be dumped into wave file real-timely, which leads that the errors can be located in time. Experimental results shows that it can improve the simulate speed remarkably.
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**References**


