SILC during NBTI Stress in PMOSFETs with Ultra-Thin SiON Gate Dielectrics

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Negative bias temperature instability (NBTI) and stress-induced leakage current (SILC) both are more serious due to the aggressive scaling lowering of devices. We investigate the SILC during NBTI stress in PMOSFETs with ultra-thin gate dielectrics. The SILC sensed range from $-1 \text{V}$ to $1 \text{V}$ is divided into four parts: the on-state SILC, the near-zero SILC, the off-state SILC sensed at lower positive voltages and the one sensed at higher positive voltages. We develop a model of tunnelling assisted by interface states and oxide bulk traps to explain the four different parts of SILC during NBTI stress.

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With the continuous scaling down of device size without reducing supply voltage appropriately, negative bias temperature instability (NBTI) becomes more serious and has been one of the most important limiting factors to PMOSFETs lifetime.\cite{1-3} Meanwhile, as the oxide thickness becomes only a few nanometres in the CMOS process now, the stress-induced leakage current (SILC) attracts more attention especially for ultra-thin gate oxide with the higher gate leakage current and with the increasing power consumption.\cite{4-6} Some authors have studied SILC and NBTI together, and provided some ideas to investigate the PMOS degradation under negative gate bias.\cite{7} In this Letter, we make a point on the gate leakage current during NBTI stress to study the mechanism and correlation of SILC and NBTI. The SILC sensed range from $-1 \text{V}$ to $1 \text{V}$ can be divided into four parts: the on-state SILC, the near-zero SILC, the off-state SILC sensed at lower positive voltages and the one sensed at higher positive voltages. Interface states and oxide bulk traps assisting tunnelling are utilized to explain the four parts of SILC during NBTI stress. Experiments at different temperatures are carried out and the results determine that the model is dependable, and indicate the correlation between SILC and NBTI.

The PMOSFETs devices used in our experiments are of surface channel. They were manufactured by a 90-nm process technology with lightly doped drain (LDD) structure and shallow trench isolation (STI) scheme. The devices have a gate width of 100 $\mu$m, and a gate length of 10 $\mu$m. The equivalent oxide thickness of the gate dielectric is about 1.4 nm with decoupled-plasma-nitridation (DPN) process. Agilent B1500A, a high-precision semiconductor parameter analyser, was used to complete the tests. Devices were stressed under the NBTI stress conditions of $V_g = V_{\text{gstress}}$ and at elevated temperatures with the source, drain and substrate grounded. Stress was interrupted at regular intervals and device parameters and the gate leakage current were measured. All stress testing were performed in a dark box.

Figure 1 shows the schematic of our experiments including NBTI stress and SILC measurement. During NBTI stress, the gate voltage is applied as stress voltage $V_{\text{gstress}} = -1.8 \text{ V}$. At interval interruptions, we extract the parameters such as threshold voltage $V_{\text{th}}$. When the gate leakage current measured, the sensed gate voltage is from $-1 \text{V}$ to $+1 \text{V}$, and other terminals are also grounded.

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of SILC can be divided into four parts: the on-state SILC, the near-zero SILC, the off-state SILC sensed at lower positive voltages and the one sensed at higher positive voltages. The positive values of SILC in Fig. 2 represent the increase of the gate leakage current compared with the initial current, and the negative values represent the descending of current. With the increase of NBTI stress time, the values of SILC sensed at positive voltage take on obvious changes. The SILC sensed at lower positive gate voltages increases with NBTI stress time while it descends at higher voltages. The value at zero of SILC exhibits larger noise due to lower gate leakage current while the near-zero values increase with time. In this study, we focus on the peaks of SILC especially at positive gate voltages.

**Fig. 2.** SILC sensed range from $-1$ V to 1 V during NBTI stress.

SILCs sensed at $V_g = 0.2$ V and $V_g = 0.6$ V to NBTI stress time are plotted in Fig. 3 with log-log scale where we have used the absolute values of SILC sensed at $V_g = 0.6$ V for easier study. The curves are both linearity, in other words, two kinds of SILC sensed at different positive gate voltages both take on power law relationship to the NBTI stress time.

**Fig. 3.** SILC during NBTI stress sensed at $V_g = 0.2$ V and $V_g = 0.6$ V.

NBTI is an effect occurring in PMOSFETs under negative gate bias stress and at high temperature. It can lead to the increase of the threshold voltage $V_{th}$ and the degradation of drain current $I_d$ and so on. The shift of threshold voltage is one of the most serious and important parameters, and many papers have studied the degradation.\cite{8-10} Figure 4 shows the relationship of the SILC sensed at $V_g = 0.2$ V and the degradation of $V_{th}$, where $V_{th}$ is extracted by the maximum slope method with drain voltage $-0.05$ V, and $V_{th0}$ is $V_{th}$ of the fresh device. The linearity between them suggests the association strongly. As the shift of threshold voltage is resulted from the generation of interface states and oxide bulk traps,\cite{11-13} there should be some connection between the degradation of gate leakage current and their generation. Therefore, we develop a model with interface states and oxide traps to explain the peaks of the gate leakage current here.

**Fig. 4.** Correlation between the SILC and the shift of $V_{th}$ of the device.

The model with interface states and oxide traps assisting tunnelling are schematically shown in Fig. 5. After NBTI stress, the devices are measured with the sensed range from $-1$ V to +1 V. When the measurement voltage is applied on the device, there are interface states and bulk traps with positive charges, which have been generated. The interface states under the Fermi level at both the interfaces of the left and right sides of oxide can be thought of as a source of electrons. When gate voltage $V_g$ is much smaller than 0 V, as shown in Fig. 5(a), the p-polysilicon valence band is higher than the n-Si conduction band. Electrons can emit from valence band and interface states under the Fermi level, which have captured electrons of p-polysilicon to the n-Si conduction band. However, as the density of electrons in p-polysilicon is very small, though there are positive charged traps assisting tunnelling, the increase of the gate leakage current is not very visible like the on-state SILC in Fig. 2. When the sensed voltage comes to near zero but still negative as shown in Fig. 5(b), there are some interface states between the Fermi level of p-polysilicon and...
body conduction band of n-Si. Therefore, electrons captured by the interface states under the Fermi level of p-polysilicon can be emitted to the interface states above the body conduction band of n-Si, and then injected into the n-Si conduction band. Taking the positive charged traps and the interface states assisting tunnelling together, there will be a small peak near zero voltage as shown in Fig. 2, the near zero SILC.

Though there are not many electrons emitted from p-polysilicon, some bulk traps can still capture some electrons to change their polarity before the sensed voltage becomes positive. The flat band voltage of our devices is about 0.18 V extracted from C-V measurement. When the gate voltage gets positive, and slightly larger than the flat band voltage, such as 0.2 V, the direction of electrons tunnelling is changed as shown in Fig. 6(a). The n-Si conduction band is slightly higher than the p-poly Si conduction band, and there are interface states between the p-polySi body conduction band and the n-Si Fermi level. Then, electrons can be injected into the interface states above the body conduction band of p-poly Si from the interface states capturing electrons under the Fermi level of n-Si, and then emitted into the p-polySi conduction band. In addition, most of the bulk traps are still positive charged though some have become negative and can play a role in lowering the barrier of electrons. In another word, they can assist the electrons tunnelling. As the n-Si is the source of electrons tunnelling, there are much more electrons than that under the condition of \( V_g < 0 \) V. Taking all the elements into consideration, there will be a much larger peak near the flat band voltage as shown in Fig. 2, the SILC sensed at lower positive voltages. When the voltage is much larger than the flat band voltage, electrons tunnel from conduction band and interface states under the Fermi level of n-Si to the p-poly Si conduction band, and the tunnelling assisted by interface states have little effect like in Fig. 6(b). With the increasing electrons captured in the oxide, more and more bulk traps become negatively charged. Then the barrier lowering of electrons tunnelling disappears. With the increasing negatively charged traps, the electron tunnelling barrier becomes higher and higher until all bulk traps become negative. Then, there will be a negative peak just as shown in Fig. 2, the SILC sensed at higher positive voltages.

In this model, the interface states and bulk traps generated during NBTI stress play an important role in the degradation of gate leakage current. However, their effect is different in different gate voltage sensed ranges. Figure 7 shows the comparison of SILC during NBTI stress sensed at \( V_g = 0.2 \) V and \( V_g = -1 \) V to fluence. We can clearly see that the degradation of gate leakage current is a factor of almost 100X higher for SILC sensed at lower positive voltage compared with that of on-state.

Figure 8 shows the SILC during NBTI stress sensed at \( V_g = 0.2 \) V at different temperatures. With the increasing temperature, the degradation of SILC becomes severe and a larger effect on SILC from the tunnelling assisted by interface states and positive charges is indicated. During NBTI stress, more interface states and positive charges are generated when the temperature becomes higher. The change in SILC with stress temperature shows that the degradation process is thermally activated. The activation energies of SILC sensed at \( V_g = 0.2 \) V and \( V_{th} \) degradation during NBTI stress can be extracted from the Arrhenius plot as shown in Fig. 9. The activation energies are 0.1168 and 0.1115, respectively. The similar activation energies show the correlation between the SILC and \( V_{th} \) degradation during NBTI stress at different temperatures, and indicate the relations to the inter-
face states and oxide charges. Therefore, it is proven that the model is dependable.

![Image](71x551 to 227x703)

**Fig. 8.** SILC during NBTI stress sensed at $V_g = 0.2\,\text{V}$ at different temperatures.

![Image](61x347 to 287x505)

**Fig. 9.** Arrhenius plot showing temperature dependence of SILC sensed at $V_g = 0.2\,\text{V}$ and $V_{th}$ degradation during NBTI stress.

In summary, we have studied the degradation of gate leakage current of PMOSFETs during NBTI stress. The SILC sensed from $-1\,\text{V}$ to $1\,\text{V}$ can be divided into four parts: the on-state SILC, the near-zero SILC, the off-state SILC sensed at lower positive voltages and the one sensed at higher positive voltages. The relationships of SILC and the NBTI time or NBTI degradation all take on regular power law. We have developed a model of tunnelling assisted by interface states and oxide bulk traps to explain the four different parts of SILC during NBTI stress. In the negative sensed voltage range, because the density of electrons in p-poly Si is very small, though there are positive charged traps assisting tunnelling, the increase of the gate leakage current is still not visible. When the sensed voltage gets near to zero, as the positive charged traps and the interface states (as shown in Fig. 5(b)) can assist electrons tunnelling, there is a small positive peak near zero voltage. When sensed voltage gets into positive voltage range, the accumulated electrons of n-Si is the source of electrons tunnelling. When the positive voltage is low, near to the flat band voltage, the tunnelling assisted by the interface states and positive charged traps (shown in Fig. 6(a)) can be taken into consideration, and a much larger positive peak will be generated. When the sensed voltage gets higher, with the increasing electrons captured in the oxide, the tunnelling assisted by interface states and bulk traps disappears. Then there will be a negative peak generated when all bulk traps become negative which makes the barrier for electrons higher. With the temperature increasing, SILC sensed at the lower positive voltage is enhanced, as there are more interface states and bulk traps that are generated and can be utilized to assist tunnelling.

**References**