Performance optimization of conventional MOS-like carbon nanotube FETs with realistic contacts based on stair-case doping strategy

Zhou Hai-liang, Zhang Min-xuan, Hao Yue

School of Computer, National University of Defense Technology, Changsha, China

School of Microelectronics, Xidian University, Xi’an, China

Due to carriers’ band-to-band tunneling (BTBT) at channel–source/drain contacts, conventional MOS-like carbon nanotube field effect transistors (C-CNFETs) suffer from ambipolar transport property. To reduce such ambipolar conductance, a stair-case doping strategy in drain lead of C-CNFETs is proposed firstly in this paper. The non-equilibrium Green’s function (NEGF)-based simulation results show that, due to the elimination of BTBT at channel–drain contacts, such stair-case doping strategy improves the OFF-state performance greatly, although the band pinning at channel–drain contact has a slight impact on the ON-state performance of the device. Then, a comparison between the performance of such doping strategy and that of previous research work has been drawn, and the simulation results reveal that this doping strategy contributes to a much greater reduction in ambipolar conductance and increase in ON–OFF current ratio, which are quite desirable in low-power applications. Further research reveals that even higher device performance can be obtained with such stair-case doping strategy adopted in both source and drain leads than just in drain lead, but at the cost of larger device area. Therefore, much attention should be paid to the choice of device structure and doping concentration to make a proper tradeoff among power, speed and area in application. At last, C-CNFETs with all kinds of realistic contacting situations are studied, and the results show that this stair-case doping strategy can improve the performance of C-CNFETs greatly even with Schottky contact taken into account.

© 2010 Elsevier Ltd. All rights reserved.

1. Introduction

In recent years, much attention has been directed to CNFETs as building blocks of nanoelectronic systems. Such interest is justified by the promise of intrinsic performance comparable to silicon-based MOSFET technology [1] and better scaling perspectives [2]. According to source/drain leads material, the contact between source/drain leads and CNT channel can be of ohmic [3] or Schottky type [4], corresponding to conventional MOS-like CNFETs and Schottky barrier carbon nanotube field effect transistors (SB-CNFETs).

Generally speaking, the Schottky barrier in SB-CNFETs contributes to the ambipolar behavior and limits the performance of these devices [4,5]. Many researches have been focused on eliminating the ambipolar behavior of SB-CNFETs. In [6], one-electron oxidizing molecules were used to obtain stable, unipolar Schottky barrier CNFETs. In [7], a horizontally laid double gate design was proposed to suppress the ambipolar behavior of SB-CNFETs. In this structure, the first gate located near the source contact was applied with gate voltage $V_g$ to control the carrier injection, and the second gate located near the drain contact was applied with the same voltage as the drain voltage or a constant voltage higher than the maximum drain voltage to suppress parasitic carrier injection. In [8], a vertically laid double gate device structure was fabricated, which exhibits n- or p-type unipolar behavior tunable by electrostatic and/or chemical doping.

All the studies introduced above are focused on SB-CNFETs. However, due to carriers’ band-to-band tunneling at channel–source/drain contacts, C-CNFETs also suffer from ambipolar transport property, which would limit the device performance largely. In order to reduce the ambipolar conductance of C-CNFETs, a linear doping strategy was proposed by Hassaninia et al. [9]. But as the simulation results showed, the obtained performance improvement was quite limited.

We must note that, however, it is just a general method to divide CNFETs into two categories, i.e. SB-CNFETs and C-CNFETs. In fact, C-CNFETs are unavoidable to be connected to metal electrodes if just one CNFET is assembled in an individual nanotube. In this case, both source and drain leads are of Schottky contact, and the
Schottky barrier at channel–source and channel–drain interfaces should be taken into account. When several CNFETs are assembled on an individual nanotube [10, 11], just Schottky barrier at channel–source (or drain) interface should be included in the simulation as for C-CNFETs with just source (or drain) lead connected to metal electrode while drain (or source) lead connected directly to another C-CNFET. As for C-CNFETs with both source and drain leads connected directly to other C-CNFETs, the source and drain leads are both of ohmic contact and no Schottky barrier should be taken into account. Of course, Schottky barriers at both channel–source and channel–drain interfaces should be considered if both source and drain leads are connected directly to metal electrodes, which is similar to that when just one C-CNFETs is assembled on an individual nanotube.

In order to obtain C-CNFETs with ideal unipolar conductance, a stair-case doping strategy is proposed in this paper. Then, the transporting characteristics of C-CNFETs with all kinds of contacting circumstances are modeled. And the simulation results show that such stair-case doping strategy can reduce the ambipolar conductance of C-CNFETs greatly, compared to the simulation results of [9].

2. Stair-case doping strategy in C-CNFETs

The considered C-CNFETs are assumed to be connected to the neighboring C-CNFETs at first. When the gate–source bias voltage (Vg) is small enough, the valence top (Ev) of channel in such C-CNFETs structure would be pulled up over the conductance bottom (Ec) of drain lead, as shown by the “Ec”–“Ev” labeled lines in Fig. 1. Holes from drain lead transport through channel–drain contact via band-to-band tunneling, as shown by the horizontal lines in Fig. 1. The resulted holes pile-up in the gated channel region contributes to its substantially deteriorated OFF-state performance and failure to support a large enough ON–OFF current ratio [12].

In order to reduce the ambipolar conductance in C-CNFETs, a novel CNFETs structure based on stair-case doping strategy, denoted by SDC-CNFETs, is proposed in this paper. And the conventional C-CNFETs structure is denoted by UDC-CNFETs for comparison. The two-dimension schematic view of the structure of SDC-CNFETs is shown in Fig. 2. Coaxial geometry, realizable in realistic application [13], is adopted for simplicity. By controlling the electrostatics of the nanotube environment by molecules [14] or metal ions [15], the left part of CNT, serving as source lead, is heavily doped with concentration of $\rho_1$, as the left “N+”-labeled rectangle shows. The middle part of CNT is left intrinsic and serves as the conducting channel as “i”-labeled rectangle shows. The drain lead is composed of two parts, the left part is lightly doped (with the concentration of $\rho_2$), while the right part is heavily doped with the same concentration as that in source lead. A coaxial gate is placed around the intrinsic part of the nanotube and separated by an oxide with thickness of 2 nm.

It must be noted that the gate bias conditions that corresponding to the beginning of BTBT depends highly on the chirality of CNT when the device under certain source–drain bias condition. The chirality of CNT is assumed to be (13, 0) in the whole work.

In this device structure, the source lead, lightly doped drain region and highly doped drain region are denoted by “S”, “D-light” and “D-heavy” respectively, and “f” represents the ratio of $\rho_2$ to $\rho_1$, i.e. $\rho_2/f = \rho_1$. Such stair-case doping profile can be achieved by using a multi-doping process such as multiple steps of modulated chemical doping [16] with appropriate exposed area at the lithography process for each step. Another technique of non-uniform doping has been reported by Alzali-Ardakani et al. [17].

3. Modeling method

Due to the wave–particle dualism, charges in CNFETs are governed by both Schrodinger and Poisson equation. Especially in nanorregion, quantum phenomena play an important role in device performance and could not be ignored any more [18, 19]. In this paper, the NEGF method is used to develop the CNFET model in order to take the quantum phenomena such as carrier tunneling and quantum capacitance into account. The NEGF formalism [20, 21], which solves Schrodinger equation and Poisson equation iteratively, provides a sound basis for quantum device simulation. In this approach, the device is described by a Hamiltonian $H_C$ using a simple $\pi$-orbital nearest neighbor tight-binding model without consideration of exchange-correlation effect. For the convenience of calculation, self-energy matrices $\Sigma_S$ and $\Sigma_D$, which provide the appropriate quantum boundary conditions, are introduced to describe the effect of source/drain leads.

Much work has been done on CNFET modeling based on NEGF method, and several CNFETs simulators have been set up. Two most famous and authentic ones are “moscnt” (set up by Guo Jing research group of Stanford University) [20] and “NANOTCAD” (set up by Gianluca Fiori research group of Pisa University) [22]. Large quantities of comparing studies show that both “NANOTCAD” and “moscnt”, which are open source, can describe the carriers transporting in CNFETs exactly [23, 24]. In order to ensure the validity of our simulation results, all the research work is carried out based on modification of “moscnt” in this paper.

4. Performance of SDC-CNFETs

With the device parameters as listed in the caption of Fig. 3, the transfer characteristic of SDC-CNFETs is shown as the black line in
Due to the stair-case doping concentration in drain lead, the corresponding band profile is of the step shape as shown in Fig. 4. When \( V_g \) is not small enough, within the range of \([-0.1 \, \text{V}, 0.04 \, \text{V}]\) in this case for instance, the band profile of D-light prevents band-to-band tunneling at drain–channel contacts from taking place. As a result, the drain current \( I_d \) of SDC-CNFETs continues decreasing, while that of UDC-CNFETs turns to increase, with the decease in \( V_g \). This would contribute to a great improvement in OFF-state performance of SDC-CNFETs as the black line in Fig. 3 shows. With the further decrease in \( V_g \), the valence top of channel would be pulled up over the conductance bottom of source lead, and the holes in source lead tunnel into channel and result in holes pile-up in channel. As a result, \( I_d \) turns to increase, after reaching a minimum of \( I_{low} \), with the decrease in \( V_g \) as the left ellipse labeled part in Fig. 3 shows.

Fig. 3. Transfer characteristics of SDC-CNFETs (black line) and UDC-CNFETs (gray line), where \( V_d = 0.4 \, \text{V}, \) oxide thickness \( t = 2 \, \text{nm}, \) channel length of 30 nm, source lead length of 20 nm, D-light length of 40 nm, D-heavy length of 20 nm, oxide dielectric \( \varepsilon = 16, \) carbon nanotube chirality of \((13, 0), \) tight-binding parameter \( V_{pp} = -3 \, \text{eV}, \) \( \rho_x = 15 \times 10^8 \, \text{m}^{-1} \) and \( f = 0.02 \) (for SDC-CNFETs).

Fig. 4. The scaled plot for the number of charges per unit energy \( (dn/dE) \) along the carbon nanotube axis in SDC-CNFETs, where \( V_g = -0.1 \, \text{V}, \) \( V_d = 0.4 \, \text{V}. \) The “Ec”- and “Ev”-denoted white lines indicate the band diagram of the first sub-band.

Fig. 5 shows the output characteristics of SDC-CNFETs and UDC-CNFETs with different gate bias conditions. When \( V_g = 0.6 \, \text{V}, \) corresponding to the ON-state, the band pinning at channel–D-light contacts, which would be introduced in detail, contributes to the current saturation as the right ellipse label part in Fig. 4 shows. As a result, the ON-state performance of SDC-CNFETs is weakened by about 0.46 orders of magnitude compared to that of UDC-CNFETs. When \( V_g = -0.1 \, \text{V}, \) corresponding to the OFF-state, the average OFF current of SDC-CNFETs is \( 4.6 \times 10^{-14}, \) about 4.7 orders of magnitude smaller than that of UDC-CNFETs, which is about \( 2.1 \times 10^{-9}. \)

Taking both the ON-state performance and OFF-state performances into account, we will find that adopting such stair-case doping strategy in drain lead of C-CNFETs can result in an increase in the ON–OFF current ratio by about four orders of magnitude but not any negative impact on the sub-threshold swing, which are quite desirable in low-power applications. However, it is known that the switching speed of a device is decided mainly by the charging and discharging speed of the output capacitance in circuit, which depends highly on the value of ON-state source–drain current. It is safe for us to conclude that the band pinning would have a negative impact on the switching speed of SDC-CNFETs. Therefore, excessive small value of \( f \) is undesired in application.

The choice of proper \( f \) value, denoted by \( f_{\text{pro}} \), is a relative complicated work owing to the fact that it is related to not only the supply voltage value, source/drain leads doping concentration but also CNT chirality. The band profile of D-light should be as high as possible in the condition of insuring the Ev in D-light lower than Ec in D-heavy. So it is easy to find that the value of \( f_{\text{pro}} \) increases with the decrease in band gap and thus the increase in chirality number “n” when CNT chirality is assumed to be \((n, 0).\)
5. Band pinning at channel–D-light contact

For a better understanding of the band pinning at channel–D-light contact, the electron distribution along carbon nanotube axis and the corresponding first sub-band profile are shown in Fig. 6.

Due to the difference in doping concentration, a depletion region exists around channel–D-light contact. When $V_g$ is small, the band profile of channel is high enough that little thermal electrons can transport into channel, where the electron density is even smaller than that in D-light, just as the solid line in Fig. 6a shows. As a result, electrons diffuse from D-light to channel as a reaction to the density gradient, resulting in an built-in electric field ($E_{in}$) pointing from D-light to channel, as the solid arrow at the bottom of Fig. 6b shows. Correspondingly, the electronic potential energy descends from left to right in the region between line “a” and line “b” in Fig. 6b. At the same time, the region between line “a” and line “c” in Fig. 6b lies within the reacting range of a outer electric field ($E_{out}$), which points from D-light to channel as the solid arrow at the top of Fig. 6b shows. So, the band profile over the whole device is of the shape as the solid lines in Fig. 6b show. Right now, the barrier height for thermal emission electrons in D-light is determined by the band profile of channel, which descends with the increase in $V_g$. So, the drain current increase with the increase in $V_g$.

With the further increase in $V_g$, the band profile of channel descends. As a result, the electron density in channel increases gradually and finally overtakes that in D-light, just as the ellipse labeled part in Fig. 6a shows. Therefore, electrons diffuse, by contraries, from channel to D-light. The resulted $E_{in}$ points from channel to D-light as the dash-dot arrow in Fig. 6b shows. Correspondingly, the band profile ascends from left to right in the region between line “a” and line “b” and then ascends due to the existence of $E_{out}$, which has the direction opposite to that of $E_{in}$. As a result, the band profile over the whole device is of the shape as the dash-dot lines in Fig. 6b show. In this case, the barrier height for thermal emission electrons in drain lead is determined by the band profile around line “b”, which is almost independent of $V_g$. In other words, the band profile at channel–D-light contact is “pinned”. As a result, current saturation takes place when $V_g$ is larger than 0.4 V.

6. Performance comparison and further optimization

As introduced in Section 1, a novel C-CNFET structure based on linear doping strategy, which is denoted by LDC-CNFETs in this paper, was proposed by Hassaninia et al. [9]. A comparison between the performance of LDC-CNFETs and that of SDC-CNFETs is shown in Fig. 7, where the transfer characteristics of LDC-CNFETs and SDC-CNFETs with $f = 0.02$ are represented by the square and triangle-marked lines, respectively. Except adopting different doping strategy in drain lead, LDC-CNFETs and SDC-CNFETs share the same device parameters. At the same time, transfer characteristic of UDC-CNFETs is also modeled as reference. Comparing the square- and triangle-marked lines in Fig. 7, we will find that, besides much higher feasibility in manufacture, a larger ON–OFF current ratio can be obtained in SDC-CNFETs than LDC-CNFETs.

ON–OFF current ratio as high as possible is one of the most important merits of ultra-low-power applications. As for SDC-CNFETs, a larger ON–OFF current ratio can be obtained by reducing the concentration of region D-light. Comparing the star-marked line to the square-marked line in Fig. 7, we will find that, with value of $f$ decreased from 0.02 to 0.01, the OFF-state performance of SDC-CNFET is improved by about 1.8 orders of magnitude.

As introduced above, the band-to-band tunneling at source-channel contact contributes to the existence of weak ambipolar conductance in SDC-CNFETs. In order to obtain even larger ON–OFF current ratio, stair-case doping strategy can be adopted in both source and drain leads. Such device structure is denoted by DSDC-CNFETs. The modeled transfer characteristic of DSDC-CNFETs is shown as the diamond-marked line in Fig. 7. Due to the elimination of a outer electric field ($E_{out}$) pointing from D-light to channel, as the solid arrow at the bottom of Fig. 6b shows. Correspondingly, the electronic potential energy descends from left to right in the region between line “a” and line “b” in Fig. 6b. At the same time, the region between line “a” and line “c” in Fig. 6b lies within the reacting range of a outer electric field ($E_{out}$), which points from D-light to channel as the solid arrow at the top of Fig. 6b shows. So, the band profile over the whole device is of the shape as the solid lines in Fig. 6b show. Right now, the barrier height for thermal emission electrons in D-light is determined by the band profile of channel, which descends with the increase in $V_g$. So, the drain current increase with the increase in $V_g$.

With the further increase in $V_g$, the band profile of channel descends. As a result, the electron density in channel increases gradually and finally overtakes that in D-light, just as the ellipse labeled part in Fig. 6a shows. Therefore, electrons diffuse, by contraries, from channel to D-light. The resulted $E_{in}$ points from channel to D-light as the dash-dot arrow in Fig. 6b shows. Correspondingly, the band profile ascends from left to right in the region between line “a” and line “b” and then ascends due to the existence of $E_{out}$, which has the direction opposite to that of $E_{in}$. As a result, the band profile over the whole device is of the shape as the dash-dot lines in Fig. 6b show. In this case, the barrier height for thermal emission electrons in drain lead is determined by the band profile around line “b”, which is almost independent of $V_g$. In other words, the band profile at channel–D-light contact is “pinned”. As a result, current saturation takes place when $V_g$ is larger than 0.4 V.

6. Performance comparison and further optimization

As introduced in Section 1, a novel C-CNFET structure based on linear doping strategy, which is denoted by LDC-CNFETs in this paper, was proposed by Hassaninia et al. [9]. A comparison between the performance of LDC-CNFETs and that of SDC-CNFETs is shown in Fig. 7, where the transfer characteristics of LDC-CNFETs and SDC-CNFETs with $f = 0.02$ are represented by the square and triangle-marked lines, respectively. Except adopting different doping strategy in drain lead, LDC-CNFETs and SDC-CNFETs share the same device parameters. At the same time, transfer characteristic of UDC-CNFETs is also modeled as reference. Comparing the square- and triangle-marked lines in Fig. 7, we will find that, besides much higher feasibility in manufacture, a larger ON–OFF current ratio can be obtained in SDC-CNFETs than LDC-CNFETs.

ON–OFF current ratio as high as possible is one of the most important merits of ultra-low-power applications. As for SDC-CNFETs, a larger ON–OFF current ratio can be obtained by reducing the concentration of region D-light. Comparing the star-marked line to the square-marked line in Fig. 7, we will find that, with value of $f$ decreased from 0.02 to 0.01, the OFF-state performance of SDC-CNFET is improved by about 1.8 orders of magnitude.

As introduced above, the band-to-band tunneling at source-channel contact contributes to the existence of weak ambipolar conductance in SDC-CNFETs. In order to obtain even larger ON–OFF current ratio, stair-case doping strategy can be adopted in both source and drain leads. Such device structure is denoted by DSDC-CNFETs. The modeled transfer characteristic of DSDC-CNFETs is shown as the diamond-marked line in Fig. 7. Due to the elimination of a outer electric field ($E_{out}$) pointing from D-light to channel, as the solid arrow at the bottom of Fig. 6b shows. Correspondingly, the electronic potential energy descends from left to right in the region between line “a” and line “b” in Fig. 6b. At the same time, the region between line “a” and line “c” in Fig. 6b lies within the reacting range of a outer electric field ($E_{out}$), which points from D-light to channel as the solid arrow at the top of Fig. 6b shows. So, the band profile over the whole device is of the shape as the solid lines in Fig. 6b show. Right now, the barrier height for thermal emission electrons in D-light is determined by the band profile of channel, which descends with the increase in $V_g$. So, the drain current increase with the increase in $V_g$.

With the further increase in $V_g$, the band profile of channel descends. As a result, the electron density in channel increases gradually and finally overtakes that in D-light, just as the ellipse labeled part in Fig. 6a shows. Therefore, electrons diffuse, by contraries, from channel to D-light. The resulted $E_{in}$ points from channel to D-light as the dash-dot arrow in Fig. 6b shows. Correspondingly, the band profile ascends from left to right in the region between line “a” and line “b” and then ascends due to the existence of $E_{out}$, which has the direction opposite to that of $E_{in}$. As a result, the band profile over the whole device is of the shape as the dash-dot lines in Fig. 6b show. In this case, the barrier height for thermal emission electrons in drain lead is determined by the band profile around line “b”, which is almost independent of $V_g$. In other words, the band profile at channel–D-light contact is “pinned”. As a result, current saturation takes place when $V_g$ is larger than 0.4 V.
of band-to-band tunneling at source–channel interface, DSDC-CNFETs is of the potential for even higher ON–OFF current ratio compared to SDC-CNFETs. But we should also notice that this would result in more serious device area cost.

7. DSDC-CNFETs with Schottky contact

As introduced above, C-CNFETs are unavoidable to contact with metal electrodes in realistic circuits even with several CNFETs assembled on an individual CNT. Therefore, DSDC-CNFETs with all kinds of realistic contacting situations are studied in this section.

Schottky barrier exists at the source/drain–CNT interface due to the work function difference between CNT and source/drain leads contact material. The Schottky barrier height, which depends highly on the choice of source/drain leads contact material are denoted by SB with DSDC-CNFETs applied with zero bias voltages, i.e. \( V_g = V_d = 0 \) V. For convenience of introduction, DSDC-CNFETs with Schottky barrier on source side, drain side or both source and drain sides are denoted by S-DSDC-CNFETs, D-DSDC-CNFETs and SD-DSDC-CNFETs, respectively.

The transfer characteristic curves of D-DSDC-CNFETs with different \( f \) and SB values are shown in Fig. 8a, where the black and gray lines represent the transfer characteristics of device doping uniform and stair-case doping strategy, respectively.

It is easy to find that, due to the suppression of holes BTBT at channel–D-light interface, the performance optimization resulted from the stair-case doping strategy is similar to that in DSDC-CNFETs with pure source and drain contacts, i.e. lower OFF-state current, higher ON–OFF current ratio and even better sub-threshold property with \( V_d \) increased from 0.4 V to 0.6 V. At the same time we will find that when \( V_g \) is relatively large enough, larger than 0.3 V for instance, the barrier height that the thermal electrons in source/drain leads faced is determined by the band profile of region S-light (lightly doped part of source lead) but not that of intrinsic part of CNT. This is similar to the band pinning at channel–D-light contact just as introduced above. As a result, a obvious reduction in ON-state current could be obtained, which is undesired in application. However, the conducting ability of a single CNT is very limited, and a bundle of CNTs are usually assembled in one CNFET in application. In this case, the conducting ability and thus the switching speed of C-CNFETs is determined by ON-state current.

Then, how about the effect of Schottky barrier at drain–metal interface? As introduced above, the performance optimization of DSDC-CNFETs is owing to the suppression of holes' band-to-band tunneling at channel–D-light interface. As minority carriers, the holes in DSDC-CNFETs are quite few. Therefore, the effect of SB value on the sub-threshold property is very limited just as shown by solid lines and dot-and-dash lines in Fig. 8a. As for the electrons transporting in DSDC-CNFETs, the Schottky barrier acts mainly as

---

**Fig. 8.** (a) The transfer characteristic curves of D-DSDC-CNFETs with different \( f \) and SB values and (b) the corresponding first sub-band profile of D-DSDC-CNFETs with \( V_g \) of 0 V, where \( V_d = 0.6 \) V, \( f = 0.01 \), oxide thickness \( t \) = 2 nm, channel length of 20 nm, heavily doped source/drain lead length of 20 nm, lightly doped source/drain lead length of 20 nm, oxide dielectric \( \varepsilon = 16 \), carbon nanotube chirality of \((13, 0)\), tight-binding parameter \( V_{pp} = -3 \) eV, \( \rho_{2D} = 15 \times 10^8 \) m\(^{-1}\).

**Fig. 9.** The transfer characteristic curves of S-DSDC-CNFETs (a) and SD-DSDC-CNFETs (b) with different \( f \) and SB values.
a additional resistance by preventing carriers in metal electrode from transporting into source/drain lead via thermal emission or tunneling just as shown in Fig. 8b. However, the band barrier for electrons in metal electrode is high enough that the effect of SB value on Id over the whole considered gate bias range is limited as well.

Similarly, the transfer characteristic curves of S-DSDC-CNFTEs and SD-DSDC-CNFTEs with different f and SB values are simulated, as Fig. 9a and b shows respectively.

What Fig. 9a and b show resemble to that of Fig. 8a in many aspects, such as the effect of stair-case doping on the transporting polarity and the effect of SB value on the sub-threshold property of the device. At the same time, we will find that the effect of SB value on Id over the whole considered gate bias range is much larger than that in D-DSDC-CNFTEs. The reason for this can be inferred from the electrons’ distribution in the device. The band barriers for electrons in metal electrodes in S-DSDC-CNFTEs or SD-DSDC-CNFTEs are much lower than that in D-DSDC-CNFTEs. The effect of SB value on the transporting electrons’ concentration in S-DSDC-CNFTEs and SD-DSDC-CNFTEs is accordingly much larger than that in D-DSDC-CNFTEs and therefore contributes to the above observed phenomenon.

8. Conclusion

In order to reduce the ambipolar conductance of C-CNFTEs, a stair-case doping strategy, which is feasible in manufacture, is proposed in this paper. Compared to that of previous related work, this stair-case doping strategy contributes to a greater reduction in ambipolar conductance and a larger increase in ON–OFF current ratio, whether the source/drain leads connected to metal electrode or not. Compared to the case where such stair-case doping strategy is only adopted in drain lead, a even much better device performance can be obtained by adopting such stair-case doping strategy in both drain and source leads. However, due to the existence of an additional lightly doped drain region, this strategy would have certain negative impacts on manufacture process and device area at the same time. So, much attention should be paid to the choice of device structure to make a proper tradeoff among power, speed and area in application.

Acknowledgment

The authors are indebted to Prof. Zoheir Kordrostami from Shiraz University for his helpful discussion and kindly help.

References

[22] [Special issue on multiscale methods for emerging technologies, N. Aluru (ed.)].