Effect of Channel Length and Width on NBTI in Ultra Deep Sub-Micron PMOSFETs

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(Received 1 August 2009)

The effects of channel length and width on the degradation of negative bias temperature instability (NBTI) are studied. With the channel length decreasing, the NBTI degradation increases. As the channel edges have more damage and latent damage for the process reasons, the device can be divided into three parts: the gate and source overlap region, the middle channel region, and the gate and drain overlap region. When the NBTI stress is applied, the non-uniform distribution of the generated defects in the three parts will be generated due to the inhomogeneous degradation. With the decreasing channel length, the channel edge regions will take up a larger ratio to the middle channel region and the degradation of NBTI is enhanced. The channel width also plays an important role in the degradation of NBTI. There is an inflection point during the decreasing channel width. There are two particular factors: the lower vertical electric field effect for the thicker gate oxide thickness of the shallow trench isolation (STI) edge and the STI mechanical stress effecting on the NBTI degradation. The former reduces and the latter intensifies the degradation. Under the mutual compromise of the both factors, when the effect of the STI mechanical stress starts to prevail over the lower vertical electric field effect with the channel width decreasing, the inflection point comes into being.


With the continuous scaling down of metal-oxide-semiconductor field-effect transistor (MOSFET) without the corresponding scaling of their supply voltages, especially when the scale gets into ultra deep region, negative bias temperature instability (NBTI) becomes more and more serious and has been one of the most important reliability problems for the state of the art CMOS technologies. NBTI is a homogeneous effect depending on the voltage applied to the gate voltage stress. Therefore, NBTI degradation is related to vertical parameters only in theory, no correlation to the lateral frame parameters. However, there are still some papers reporting that the channel length and width can affect the sensitivity of the temperature instability, and there is no uniform idea for the effect of the two lateral frame parameters on NBTI. Cellere et al. discussed the NBTI dependence on channel length and width and thought that the devices with shorter and wider channel are the most sensitive to NBTI. Jin et al. reported that the enhanced interface trap generation near the gate edge is primarily responsible for the channel length dependence of NBTI degradation and BF3 lightly doped drain (LDD) can suppress the non-uniform distribution of interface traps along the channel. Steve et al. thought that the shallow trench isolation (STI) can make an important role in the degradation of NBTI and enhance the effect as a reduction of the gate width. However, with the scaling of the device, the need have a comprehensive and microcosmic study on the effect of the channel length and width on NBTI is more and more urgent. In this Letter, we study the degradation of different lengths and widths devices, and make an analysis on the mechanism.

The PMOSFETs used here are of surface channel. They were manufactured using a 90 nm process technology with lightly doped drain (LDD) structure and STI scheme. The gate oxides of all devices were annealed in N2O atmosphere after thermal growth. There are two series of devices used here, which have the same gate oxide thickness of 1.4 nm. One series have the same gate width 10 µm with different gate lengths from 0.09 µm to 1 µm and the other has the same gate length 0.1 µm with different gate widths. Agilent B1500A, a high precision semiconductor parameter analyzer was used to perform the tests. Gate voltage stress is supplied to be \( V_{gd} = V_{gstress} \) with \( V_d = V_s = V_{sub} = 0 \) at elevated temperatures. Stress was interrupted at regular intervals and the threshold voltage \( V_{th} \) is measured and used to present the degradation of NBTI as it is the most degraded parameter.

In the experiments, we make the devices with different channel lengths stressed under NBTI stress to study the effect of the channel length on the degradation. Figure 1 shows the threshold voltage shift of the devices with different channel lengths as a function of...
stressing time when gate bias stress \( V_{\text{gstress}} = -2.0 \text{ V} \) is applied at \( T = 120^\circ\text{C} \). With the variation of length from 1 \( \mu\text{m} \) to 0.09 \( \mu\text{m} \), the degradation of \( V_{\text{th}} \) is increasing. All \( V_{\text{th}} \) shifts show good logarithmic relation to the stress time and exhibit similar degradation tendency.

![Fig. 1. Threshold voltage shift as a function of stress time under NBTI stress with channel lengths.](image1)

The threshold voltage shift as a function of channel length under NBTI stress is plotted in Fig. 2. From Fig. 2, we can see that the channel length affects the threshold voltage shift seriously. With the decreasing channel length, the degradation of NBTI increases, which shows an approximate logarithmic relation and implies an inhomogeneous effect during the NBTI stress. This effect cannot be caused by the lateral electric field, which is always responsible for the non-uniform damage in the device[10−11] as there is no potential drop along the channel. Therefore, the results due to the inhomogeneous effect may be resulted from the non-uniform distribution of the defects.[6]

Though gate voltage stress is applied only and supplies a uniform stress electric field along the channel, there is still non-uniform degradation effect. This result may be resulted from the inhomogeneous distribution of the damage among the gate and source/drain overlaps and the middle channel regions. The gate edge regions are most likely to be damaged during the fabrication process, such as the implantation and the etch processes.[12] The related species which can cause latent damage such as water, hydrogen and boron can diffuse from the gate edge into the gate oxide and result in more damage.[7,13−14] Therefore, there are more damage and latent damage in the gate edge regions, namely, the overlaps of the gate and source/drain regions than the middle channel regions.

Figure 3 presents the schematic diagram showing the non-uniform distribution of damage in three parts of the PMOSFET: the gate and source overlap region \( L_{gs} \), the middle channel region \( L_{mc} \), and the gate and drain overlap region \( L_{gd} \). As the same fabrication is used and the same bias is stressed, the both edge regions are independent of the channel length. We suppose the ratio \( r = (L_{gs} + L_{gd})/L_{mc} \), in which the denotations have explained above. When the channel length decreases, \( L_{mc} \) becomes smaller and the ratio \( r \) becomes larger. During NBTI stress, interface traps are generated and shift the threshold voltage and other parameters. The origin of the interface traps is the breaking of the weak bond of Si formed with H or B. As there are more related species which can lead latent damage in the channel edge regions, the both edge regions will result into larger degradation than that of the middle channel region. Therefore, with the channel length decreasing, the edge regions play a more important role as the ratio \( r \) becomes larger, and then result in a more serious degradation under the same NBTI stress as observed in Fig. 2.

![Fig. 2. The threshold voltage shift as a function of channel length under NBTI stress.](image2)

![Fig. 3. The schematic diagram showing the non-uniform distribution of damage in three parts.](image3)

![Fig. 4. The ratio of the difference of the extracted gate voltages with higher drain voltages to that with -0.05 V drain voltage (a) the ratio of forward and reverse (making the source as drain) (b) as a function of measurement drain bias.](image4)

To support the claim above, we use the detection measurement to see the gate voltage differences when the drain current reaches a standard current value.
The devices with different channel widths are stressed under NBTI stress to study the effect of the channel width on the NBTI degradation. The gate bias stress $V_{\text{stress}} = -1.8 \, \text{V}$ is applied to the devices at $T = 90^\circ\text{C}$. From the experimental results, we find that with the width varying from 100 $\mu\text{m}$ to 0.4 $\mu\text{m}$, the degradation of $V_{\text{th}}$ appears an extremum point and $V_{\text{th}}$ shifts of all devices show power law to the stress time and exhibit similar degradation tendency.
Fig. 7. Sub-threshold slop shift of degradation under NBTI stress in devices with different widths.

Figure 7 shows the sub-threshold slop of devices with different widths as a function of stress time. The device with 0.4 μm has a more degradation of the sub-threshold slop than that of the other devices which shows the interface traps play a more important role in the ultra narrow devices and improves the claim above.

In summary, we have made a point on the effects of channel length and width on the degradation of NBTI. With the channel length decreasing, the degradation of NBTI increases. The two regions of the channel edge have more damage and latent damage for the process reasons. Then, when the NBTI stress is applied, there will be inhomogeneous degradation generated which leads to the non-uniform distribution of the generated defects in the three parts. The shorter the channel length, the larger the ratio \( r \), the more important role the channel edge regions can play, and the larger the degradation of NBTI. When the channel width comes into consideration, there is an inflection point comes into being during the decreasing channel width. As there are two factors in particular: the lower vertical electric field effect for the thicker gate oxide thickness of the STI edge, and the STI mechanical stress. The former reduces and the latter intensifies the degradation. Under the mutual compromise of the both factors, when the effect of the STI mechanical stress on the device starts to prevail over the lower vertical electric field effect with the channel width decreasing, the inflection point is generated.

References