Performance and Power Analysis of Long Line Interconnection Torus networks for Network-on-Chips

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Abstract: With increasing scale of Network-on-Chips (NoCs), the power caused by long line wires between cores counts for a significant proportion of the NoCs energy consumption. Most of the study on NoCs topologies assumes that interconnect wires between cores are same length and are short lines. Taking 2D 4×4 torus network as an example in this paper, we present a long line interconnects network model for analyzing latency and energy consumption of NoCs. Simulation shows the different between this model and short line model. We also propose a novel approach based on low swing circuit using MOS current mode logic (MCML) to decreasing power consumption of long line wires in NoCs. Compared to the conventional full swing circuit, Simulation results show that the total NoCs link energy consumption can be reduced.

Keywords: Long line, torus network, MCML

1. Introduction
With the advance of the semiconductor technology, the enormous number of transistors available on a single chip allows designers to integrate dozens of IP (Intellectual Property) blocks. Network-on-Chips (NoCs) are a promising approach to handle the growing problems of SoCs caused by the increasing number of components on a single chip [1]. The main advantages of Network-on-Chips are the regularity of the inter-connection network, the reduction of electromagnetic effects, and the good scalability [2].

The performance of a NoCs is determined by a variety of factors, one of which is the network topology [3]. The choice of network topology has significant impact on the communication and the performance of the entire NoC. The 2D mesh topology is one of common topologies in designing NoCs because it is simple and also compatible with the basic 2D nature. Compared with 2D mesh, 2D torus structure has better network performance [4]. In the 2D torus structure, nodes at the edges are connected to the nodes at the opposite edge through wraparound channels. Long line wraparound channels will greatly increase the delay and power consumption of NoCs.

In this paper, we compare the difference between long line and short line model, and then a new low swing differential signaling circuit is proposed to reduce power consumption of 2D torus network in long line model.

2. Long line 2D Torus network model

Most of the study on NoCs topologies assume that interconnect lines between cores are same length, and the interconnect wires are short line [5] [6]. On this basis, research the performance or power of NoCs. However, a significant amount of power is dissipated on long line interconnects in 2D torus network. Neglecting the long line interconnects will lead to study results inaccurate. The delay of the long interconnects wires are quadratic to linear. Traditional method is insertion of repeaters to decrease the delay. In spite of its simplicity and popularity, repeater insertion scheme counts for a significant proportion of the NoCs energy consumption [7]. In engineering practice, there are performance and cost trade-offs between delay and the number repeater. It means that the performance of the NoCs based on torus network can not reach indices which analyzed by traditional short line model. To analyze torus network model, a more accurate method is necessary.

In this section, we present our long line 2D torus network model. Fig.1 is a 4×4 long line torus model, the node Rdt are routers, and PE are processing elements. Throughout this paper, we use Rdt to distinguish the different R node, where 0≤d≤3 and 0≤t≤3. Besides, the edges are denoted by L(d1, d2), where 0≤d1, d2 ≤3 and 0≤t1, t2≤3. In this model, the set of long line interconnects is denoted by \{L(d1, t1)| 0≤d, d1≤3, t1=0 or 0≤t1≤t2≤3,d2=3, d1=0\}.
2.1 Router structure
We assume the router has 5 input/output ports, with 2 VC (Virtual Channel) per input port; a crossbar and a arbiter. Routers receive packets on their input ports and after routing a packet based on the routing algorithm and destination address, the packet is sent to the selected output port.

Fig. 2. Router model
Fig.2 shows internal structure of a router node. LinkN, LinkS, LinkE, LinkW represent 4 input/output channels from neighbor routers, respectively. MUX and DEMUX handle the virtual channel operations. Crossbar switch directly connects each input channel to each unoccupied output channel. Arbiter controls the crossbar switch and other related sub-modules.

2.2 Routing algorithms
Routing algorithms establish the path between the source and destination nodes. In order to simplify the analysis, we use XY-routing algorithm in our long line 2D 4×4 torus network model. XY-routing is a non-adaptive routing algorithm which is widely used in mesh NoCs model. According to this algorithm, packets first along the x-dimension and then along the y-dimension until the packet reaches the destination.

3. Low swing circuit using MCML
Long line interconnects increases the delay of the signal. Inserting repeaters is a widely used method to decrease the delay of the long interconnects wires. Repeater insertion scheme counts for a significant proportion of the total chip energy consumption, so the low swing interconnect technology is introduced to decrease the energy consumed on the interconnect wires.

The dynamic energy of the interconnect is expressed as

\[ P_{\text{dyn}} = \alpha \cdot C_i \cdot V_{dd} \cdot V_{\text{swing}} \cdot f_{\text{link}} \]  

(1)

\( P_{\text{dyn}} \) is primarily due to charging and discharging of capacitive loads (wire and input capacitance of next stage repeater). \( \alpha, V_{dd}, V_{\text{swing}} \) and \( f_{\text{link}} \) denote the link activity factor, supply voltage, signal swing voltage and frequency respectively, and \( C_i \) is load capacitance. From the equation (1) it is seen that lowering the voltage swing on interconnect wires the interconnect energy dissipation can be decreased by lowering the voltage swing on interconnect wires. The energy saving ratio is

\[ \frac{E_{\text{saving}}}{E_{\text{following}}} = \frac{V_{\text{saving}}}{V_{dd}} \]  

(2)

To decrease the transmission energy consumption between PE cores, the driver converts the full swing signaling into low swing signaling at the beginning of the long line wires, and the receiver converts the voltage swing back to full swing at the end of the long line wires.

Traditional low swing drivers use reference voltages or use the threshold voltage of the MOSFET to limit the signal swing. The reference voltage generator will introduce extra energy consumption and layout area, and the utilization of threshold voltage can not get an ultra low swing. The Low swing circuit using MOS current mode logic (MCML) \([8]\) doesn’t require any additional reference voltage when the input full swing voltage signaling is converted into a low swing signaling. If the swing becomes much lower, the noise immunity of the single-ended circuit decreases. The circuit (Fig.3) consists of a simple MOS current mode logic circuit and an inverter. The MOS current mode logic (MCML) circuit includes a current source, a differential pull-down network and the active pMOS loads. With differential inputs and outputs, the circuit has robust noise immunity. The driver circuit has constant energy consumption, because of the use of a constant current source.

4. Simulation Results and Analysis
We introduce some assumptions and definitions used in our simulation.

(1) In short line 2D torus network model, the wire length is 1mm and the interconnect wires between PE cores are same length. The transmission rate is 1 Gbps.

(2) Considering the limitation of NoCs area and energy consumption, in long line 2D torus network model, long line wire length is 10mm and 2 repeaters are used. The transmission rate is 250 Mbps.

The simulation result of average packet latency between short line model and proposed model is shown in Fig.4.
Fig. 4. A comparison in average packet latency between short line model and proposed model. Because of the tradeoff between bandwidth and energy consumption of long line, it can be seen that the proposed model having poorer throughput than short line with XY-routing algorithm. Compared with traditional short line model, this result is more tally with the actual situation.

Fig. 5. Long line interconnect model using MCML. A simulation is also made between repeater insertion and MCML low swing in long line 2D torus network model. In the simulation, we used 0.18μm CMOS technology. The interconnect wires is 0.56μm width and 0.28μm spacing. MCML Long line wires is modeled by an n3 distributed RC model (Fig. 5).

Fig. 6. A comparison in link energy between repeater insertion and MCML low swing wire length. Long line interconnect wire length is changed from a 6mm to 15mm. Link dynamic power $P_{\text{dyna}}$ is calculated by equation (1), and $C_l$ is expressed as

$$C_l = C_{\text{in}} + C_{\text{ground}} + C_{\text{cc}}$$

(3)

Where $C_{\text{in}}$ is the input capacitance of the next repeater, $C_{\text{ground}}$ is the ground capacitance and $C_{\text{cc}}$ is coupling capacitances of the wire driven. Simulation results are shown in Fig. 6, it shows that with the long line interconnect wire length growing longer, the link energy consumption of NoCs using MCML low swing scheme becomes much lower than that of the repeater insertion scheme. And the layout area of the NoCs using MCML low swing scheme is much smaller than that of the repeater insertion scheme. So MCML low swing circuit is a promising scheme for the NoCs long line interconnects.

5. Summary

Obtaining an estimation of the NoCs performance is a significant parameter at early design phases. Network model is an effective approach to address this issue. In this paper, we proposed long line interconnects NoCs model. Simulation results shows that proposed model is more tally with the actual situation. Comparison between repeater insertion and MCML low swing circuit show that the MCML low swing circuit can decrease the total interconnection energy substantially of NoCs, and the layout is small. So it is an efficient method to decrease NoCs link energy consumption.

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References